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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/047,518	Applicant(s) HUANG, YISHAO MAX	
	Examiner Tanh Q. Nguyen	Art Unit 2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2001 and 04 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6, 9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 14-30 are objected to because of the following informalities:

"devices operable" in line 3 of claim 14 should be corrected to "devices **are** operable".

"comprising configuration" in line 2 of claim 24 should be corrected to "**comprises** configuration"

"rout" in line 2 of claim 26 is misspelled.

"first or second input/output paths" in line 3 of claim 26 should be corrected to "first or second input/output **path**".

"first and second input/output path" in line 4 of claim 27 should be corrected to "first and second input/output **paths**".

"first or second embedded devices" in line 5 of claim 27 should be corrected to "first or second embedded **device**".

"wherein said first embedded device selected from" in line 2 of claim 28 should be corrected to "wherein said first embedded device **is** selected from".

"first or second input/output paths" in line 4 of claim 27 should be corrected to "first or second input/output **path**".

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 14-26, 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 14-26 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: "a single bus slot" is recited in both line 1 and line 3 of claim 14, suggesting that the single bus slot in line 1 is not the same as the single bus slot in line 3. It is therefore not clear which bus "said bus" in line 5 of claim 14 refers to. For purpose of examination, claim 14 is interpreted to have one single bus slot (i.e. a PCI bus slot).

5. Claim 26 recites the limitation "said processor" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: claim 27 recites a first embedded device, a second embedded device, and an expansion card device and claim 30, which depends on claim 27, recites "said device" in line 2. It is therefore

not clear which device "said device" refers to. For purpose of examination, "said device" in claim 30 is interpreted as the expansion card device.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 14-16, 18-21, 23, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by **Emerson et al. (USP 6,664,969)**.

9. As per claim 14, **Emerson** teaches an integrated expansion card [50, FIG. 2 and FIG. 3] occupying a single bus slot [16, 20, FIG. 2; 16, FIG. 3; col. 5, lines 9-10] of a computer system [S, FIG. 1], comprising;

a first embedded device [114A, 118A, FIG. 3] and a second embedded device [111, FIG. 3] wherein said first and second embedded devices are operable to share the single bus slot (col. 5, lines 46-52: the first embedded device sharing the single bus slot; col. 3, lines 60-62: the second embedded device necessarily sharing the single bus slot to provide functionality for accessing, interacting and monitoring the managed server S from remote console C), said second embedded device comprising a bus host controller

[111, FIG. 3] operable to input and output commands and data to said bus [16, FIG. 3; col. 3, lines 60-62] and to an expansion card device [112A, FIG. 3] connected to said host bus controller (col. 5, line 9-col. 6, line 23).

10. As per claims 15-16, 18-21, 23, 25, Emerson teaches the first embedded device comprising a video controller [114A, FIG. 3];

the first embedded device comprising a network controller [110, FIG. 3];

the first embedded device comprising a memory device [106, 108, 118A, FIG. 3];

the first embedded device comprising a core logic chipset associated with said computer system [100, 116A, FIG. 3];

a PCI bus [16, FIG. 3], a PCI bus slot for physically connecting the expansion card to the computer system (col. 5, lines 9-10);

the second embedded device comprising a PCI-to-PCMCIA host controller [111, FIG. 3];

a processor [100, FIG. 3] to connect the input and output of said first and second embedded devices and the expansion card device to the PCI bus (col. 5, line 9-col. 6, line 23);

the expansion card comprising a first input/output path [111-100-16, FIG. 3] and a second input/output path [114A-100-16, FIG. 3] for communication between said first and second embedded devices, respectively, with said computer system.

11. Claims 14, 16, 19, 20, 23-24, 25 are rejected under 35 U.S.C. 102(e) as being anticipated by **Kamepalli (USP 6,647,434)**.

12. As per claim 14, 23-24, **Kamepalli** teaches an integrated expansion card [121, FIG. 2] occupying a single bus slot [125, FIG. 1; 123, FIG. 2; col. 3, lines 38-40] of a computer system [101, FIG. 1], comprising;

a first embedded device [F0-F7, FIG. 2] and a second embedded device [F0-F7, FIG. 2] wherein said first and second embedded devices are operable to share the single bus slot, said second embedded device comprising a bus host controller [SCSI CONTROLLER, ETHERNET CONTROLLER, FIG. 2] operable to input and output commands and data to said bus [123, FIG. 2] and to an expansion card device [SCSI BUS device, ETHERNET connector, FIG. 2] connected to said host bus controller; and

a processor [207, FIG. 2] to connect the input and output of the first and second embedded devices and the expansion card device to the PCI bus, wherein the processor comprises configuration registers [FIG. 3] comprising a header region [00h-3Ch, FIG. 3] and a device dependent region [40h-FFh] for each embedded device, said header region comprising data to identify the embedded devices and device dependent region comprising data specific to the first or second embedded device (col. 3, lines 55-col. 4, line 5).

13. As per claims 16, 19, 20, 25, Kamepalli teaches the first embedded device comprising a network controller [F3-F5, FIG. 2];

the first embedded device comprising a core logic chipset associated with the computer system [205, 207, FIG. 2];

a PCI bus [123, FIG. 3], a PCI bus slot [125, FIG. 1] for physically connecting the expansion card to the computer system (col. 3, lines 38-40);

the expansion card comprising a first input/output path [one of F0-F7 to 205, FIG. 2] and a second input/output path [a different one of F0-F7 to 205, FIG. 2] for communication between said first and second embedded devices, respectively, with the computer system.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 17, 22, 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Emerson et al.**.

16. As per claim 17, Emerson does not specifically teach the first embedded device comprising a modem. Emerson, however, teaches other communications devices being used as required by the network type (col. 5, lines 41-43), and a modem [112A, FIG. 3] being preferably coupled to the PCI bus 102 with a PCI-PCMCIA bridge (col. 5, lines 43-45), hence suggests to one of ordinary skill in the art that a PCI-compliant modem can be connected to the PCI bus 102, in the same manner as the PCI-compliant network

controller [110, FIG. 3] for the purpose of allowing remote access to the computer system [S, FIG. 1] in an alternate embodiment.

17. As per claim 22, Emerson does not specifically teach the expansion card device comprising a smart card reader. Emerson, however, teaches a PCI-PCMCIA bridge [111, FIG. 3] and a card reader [112A, FIG. 3]. Since it was well known in the art at the time the invention was made for a smart card reader to be implemented through a PCI-PCMCIA adapter and a PCMCIA smart card reader, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the presence of a PCI-PCMCIA bridge in Emerson's integrated expansion card would allow for connection of a PCMCIA card reader to Emerson's integrated expansion card, such connection allowing the computer system [S, FIG. 1] to interact with a smart card reader and access a smart card.

18. As per claim 26, Emerson does not specifically teach a function router comprising a multiplexer to route data and control signals between a processor and the first or second input/output path. Emerson, however, teaches an arbitration unit being included in the processor [100, FIG. 3; col. 5, lines 27-28], hence the arbitration unit directing data and control signals between the internal PCI bus [102, FIG. 3] of the integrated expansion card and the external PCI bus [16, FIG. 3].

Emerson further teaches a plurality of functions (a network function, a PCI-PCMCIA function, a remote management function, a video function,...) sharing a single PCI bus slot [16, FIG. 3]. Since Emerson's integrated expansion card [50, FIG. 3]

effectively replaces the plurality of required PCI bus connections corresponding to the plurality of functions (according to the PCI bus specification) with a single PCI bus connection [16, FIG. 3], it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a function router for the purpose of routing data control and control signals between the different functions (embedded devices) and the single PCI bus connection [16, FIG. 3] in conformance with the PCI bus specification - hence a function router to route data and control signals between the single PCI bus connection [16, FIG. 3] and the first or second input/output path.

Furthermore, it was well known in the art at the time the invention was made for a PCI bus - in compliance with the PCI specification - to be a multiplexed bus, such that address signals and data signals share the same physical lines. It would have been obvious to one of ordinary skill in the art at the time the invention was made for Emerson's integrated expansion card to include a router comprising a multiplexer - for the purpose of routing data control and control signals between the different functions (embedded devices) and the single PCI bus connection [16, FIG. 3], and adhering to the PCI bus specification to multiplex data and control signals between the single PCI bus connection [16, FIG. 3] and the embedded devices.

19. As per claims 27-30, see the rejections to claims 14-21, 25-26 above. Emerson further teaches the PCI-PCMCIA controller being a PCI-PCMCIA bridge [111, FIG. 3]

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tanh Quang Nguyen whose telephone number is (703) 305-0138, and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 for After Final, Official, and Customer Services, or (703) 746-5672 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

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March 17, 2004